

S/N TBD
Docket: CS03-050
Group art unit : ___ TBD

Date 01/21/2004

To: Commissioner of Patents and Trademarks
P.O. Box 1450 Alexandria, VA 22313-1450

Fr: William J. Stoffel Reg. No. 39,390 CUST NO. 30402
PMB 455
1735 Market St - Suite A
Philadelphia, PA 19103

Subject:

Serial No. TBD
Docket **CS03**-050
File Date: with application
Inventor: Chui et al.

**title: STRUCTURE AND METHOD TO FORM SOURCE AND DRAIN
REGIONS OVER DEPLETION DOPED REGIONS**

Group art unit: TBD

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO A820 (also PTO-1449), Information
Disclosure Citation and references.

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William J. Stoffel Reg. No. 39,390
Customer number 30402

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The following Patents and/or Publication are submitted to comply with the duty to disclose under CFR 1.97-1.99 and 37 CFR 1.56.

US 6,383,883B1 (Chen et al.) shows a graded S/D region.

US 6,348,372B1 (Burr) shows a Method to reduce S/D junction capacitance.

US 2003/0132452 A1 (Boriuchi) shows a recombination region.

US 5,795,803 (Takamura et al.) shows a well process.

US 6,528,826B2 (Yoshida et al.) shows a device.

US 2002-009364A1 (Inaba) shows a semiconductor device.

US 5,712,204 (Horiuchi) shows a method for S/D regions.

Inaba, et al., "Silicon on Depletion layer FET (SODEL FET) for sub-50 nm high performance CMOS applicaiotns: novel channel and S/D profile engineering schemes by selective Si epitaxial growth technology".., 2002, IEEE.

Sincerely,



William J. Stoffel
Reg. No. 39,390
Customer number 30,402

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Application Number	
Filing Date	
First Named Inventor	CHDI
Art Unit	
Examiner Name	
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U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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Application Number					
	Filing Date				
	First Named Inventor chui				
	Art Unit				
	Examiner Name				
Sheet	2	of	2	Attorney Docket Number	cs03-050

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Inaba, et al., "silicon on depletion layer FET (SODEL FET) for sub - 50 nm high performance... by selective Si epi growth technology, 2002, IEEE	

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